PAPER

Single event effect hardness for the front-end ASICs in the DAMPE satellite BGO calorimeter

Single event effect hardness for the front-end ASICs in the DAMPE satellite BGO calorimeter *

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Abstract: The Dark Matter Particle Explorer (DAMPE) is a Chinese scientific satellite designed for cosmic ray studies with a primary scientific goal of indirect detection of dark matter particles. As a crucial sub-detector, the BGO calorimeter measures the energy spectrum of cosmic rays in the energy range from 5 GeV to 10 TeV. In order to implement high-density front-end electronics (FEE) with the ability to measure 1848 signals from 616 photomultiplier tubes on the strictly constrained satellite platform, two kinds of 32-channel front-end ASICs, VA160 and VATA160, are customized. However, a space mission period of more than 3 years makes single event effects (SEEs) become threats to reliability. In order to evaluate SEE sensitivities of these chips and verify the effectiveness of mitigation methods, a series of laser-induced and heavy ion-induced SEE tests were performed. Benefiting from the single event latch-up (SEL) protection circuit for power supply, the triple module redundancy (TMR) technology for the configuration registers and the optimized sequential design for the data acquisition process, 52 VA160 chips and 32 VATA160 chips have been applied in the flight model of the BGO calorimeter with radiation hardness assurance.

Keywords: space electronics, single event effects, radiation hardness, heavy ion, pulsed laser

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1 Introduction

DAMPE (Dark Matter Particle Explorer), one of the four satellites supported by the Strategic Priority Research Program on Space Science of the Chinese Academy of Sciences, is planned to be launched at the end of 2015. Its main scientific objective is to measure cosmic rays with a much wider energy range (5 GeV–10 TeV) than existing space experiments, in order to identify possible dark matter signatures [1].

As a key sub-detector of DAMPE, the BGO (Bismuth Germanate) electromagnetic calorimeter provides a wide range of energy deposition of particles traversing the detector. In order to reconstruct the electromagnetic shower profile, 308 BGO crystal bars with dimensions of 2.5 cm × 2.5 cm × 60 cm form 14 layers. Crystal bars in consecutive layers are oriented orthogonally to each other. Each crystal bar optically couples two Hamamatsu R5610 photomultiplier tubes (PMTs). The 2nd, 5th and 8th dynodes of each PMT are measured synchronously to achieve a total dynamic range of 2×10^5 [2, 3]. Hence, to measure 1848 signals on the power-limited and weight-limited satellite platform, two readout chips for PMTs (VA160 and VATA160), are customized to implement high-density and low-power front-end electronics (FEE) [4].

However, single event effects (SEEs) are vital factors that affect the reliability of the FEE [5]. DAMPE will orbit the earth at an attitude of 500 kilometers and an inclination of 97° for the mission period of at least 3 years. Radiation sources of the orbit are composed of galactic cosmic rays, solar particles, and particles trapped in the Van Allen belts, which results in a wide variety of particles with various amounts of kinetic energy corresponding to a wide spectrum of linear energy transfer (LET). Through CREME96, a tool for SEE rate prediction, the LET spectrum of the orbit is calculated, as shown in Fig. 1 [6]. It indicates that the SEE tolerance of the semiconductor should be greater than 37.5 MeV·cm^2/mg, otherwise mitigation methods should be seriously considered to assure radiation hardness.

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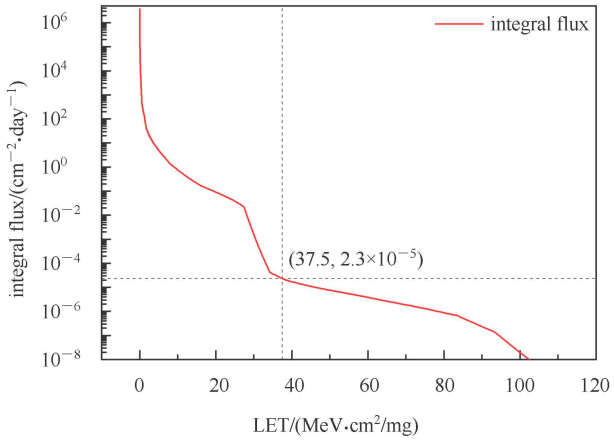

Fig. 1. (color online) The integral LET spectrum for silicon (calculated by CREME96).

2 Overview of VA160 and VATA160

VA160 and VATA160 chips, which are designed by IDEAS (Norway) and manufactured with the 0.35 μm CMOS technology processed on epitaxial silicon wafer, are able to cope with 32 channels of PMT dynode signals simultaneously. The die of the VATA160 chip is composed of two independent functional parts, as shown in Fig. 2, the left part is called the VA part and the right part is called the TA part. The VA part, which is exactly the same as the die of the VA160 chip, consists of 32 identical channels for charge measurement [7]. The charge pulse from the PMT dynode is fast amplified by a charge sensitive amplifier (CSA), shaped by a slow shaper (S), sampled by a sample-and-hold unit (S/H), and switched to a differential current output buffer (AOB) via an analogue multiplexer (AMUX). Besides, via the analogue de-multiplexer (ADEMUX), each channel can be calibrated by injecting the external calibration charge. The TA part generates trigger information. The output of each CSA is directly coupled to the corresponding input of the TA part. It is amplified via a programmable gain stage (G) and a fast shaping amplifier (FS), then discriminated by a low-sensitive discriminator (C). If the pulse height exceeds the common threshold, a trigger signal is generated. All channels share a common wire-ORed trigger output. There are a few digital circuits in these chips as well. Two 32-bit shift registers of the VA part control AMUX and ADEMUX respectively. A 165-bit configuration register of the TA part stores the operating settings.

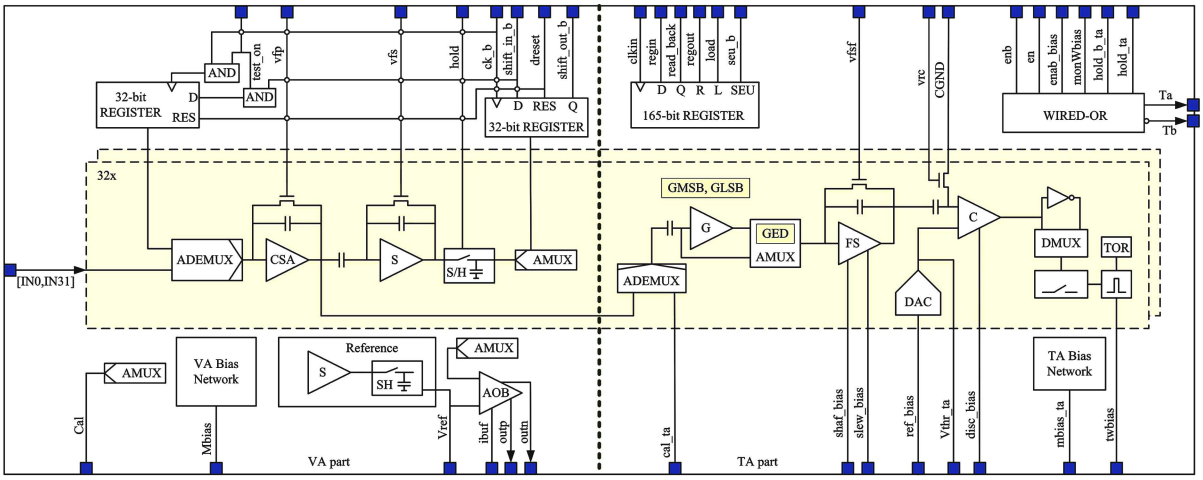

Fig. 2. (color online) The architecture of VATA160.

3 Experimental approaches and results

3.1 Test setup

In order to fit different irradiation facilities, the test setup shown in Fig. 3 was designed. Apart from the device under test (DUT), the DUT board includes a few passive components and connectors which are radiation-insensitive. VA160 and VATA160 have their own DUT boards. The DAQ board is much like a special IC tester designed for irradiation tests. It supplies power, sets work mode, monitors operating current, measures performance, and distinguishes abnormalities for the DUT. An acquisition program on the remote computer controls the DAQ board via a RS-485 bus.

3.2 Laser-induced SEE testing

Laser-induced SEE testing is a much more cost-efficient way to rehearse heavy ion testing and verify the effectiveness of mitigation methods. Tests were performed at the Pulsed Laser Single Event Effects Facility (PLSEE) in the National Space Science Center (Beijing).

A pulsed laser with wavelength 1064 nm scanned the entire chip to explore latch-up phenomena [8].

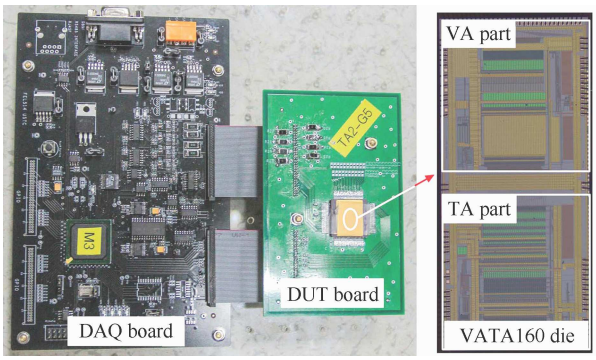

Fig. 3. (color online) The test setup and the die of VATA160.

Some interesting results were obtained. Firstly, as the spot diameter of the laser beam was less than 3 μm, observable latch-up sensitive areas were precisely located. Figure 4 shows some of them. Secondly, the minimum laser energy triggering latch-up of the VA part (or VA160) was greater than that of the TA part, which implies that the threshold LET of the VATA160 is lower. Thirdly, once a sensitive area was triggered, the current rose immediately to a steady value thereafter even though the same position was still under exposure. If the laser continued to irradiate other sensitive areas, the current raised step-by-step until the power shut off. However, the pulsed laser is different from heavy ions in its mechanism of energy deposition, and the forward incident laser can hardly reach the sensitive areas covered by the metal layers, so heavy ion testing is indispensable [9].

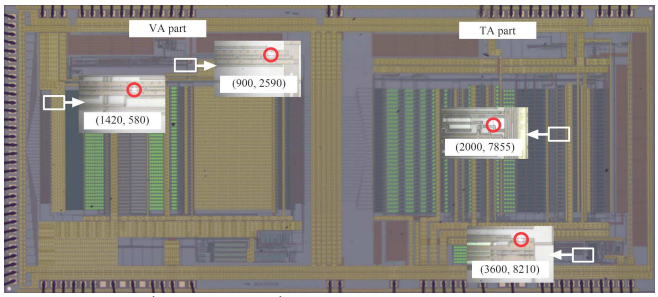

Fig. 4. (color online) Some SEL sensitive areas obtained from the laser testing.

3.3 Heavy ion-induced testing

Heavy ion tests were performed at the Heavy Ion Research Facility in Lanzhou (HIRFL, Lanzhou) and HI-13 tandem accelerator at the China Institute of Atomic Energy (HI-13, Beijing). The irradiation tests performed at HIRFL were in air. It was convenient to observe all abnormal phenomena induced by ion strikes. However, changing species or initial energy of ions is time-consuming, so degraders were preferred to adjust the ion energy on the surface of the die and thus specified LET values were obtained. Irradiation tests performed at HI-13 were in vacuum. DUT boards mounted inside the vacuum chamber were connected with DAQ boards through special adapters on the chamber. Since the number of adapters is limited, only power lines for DUTs were connected to investigate SEL. Five VA160 chips and three VATA160 chips with removal of the package lids were tested.

The test results of SEL are summarized in Table 1. In order to get saturated cross section ($\sigma_{\rm sat}$), threshold LET ($\rm LET_{th}$), width factor (W) and shape factor (S), Weibull distributions are fitted for VA160 and VATA160 in Fig. 5 and Fig. 6 respectively. With these four parameters and the LET spectrum, SEL rates due to direct ionization are calculated to be: 7.5×10^{-5} /device/day for VA160 and 5.2×10^{-4} /device/day for VATA160.

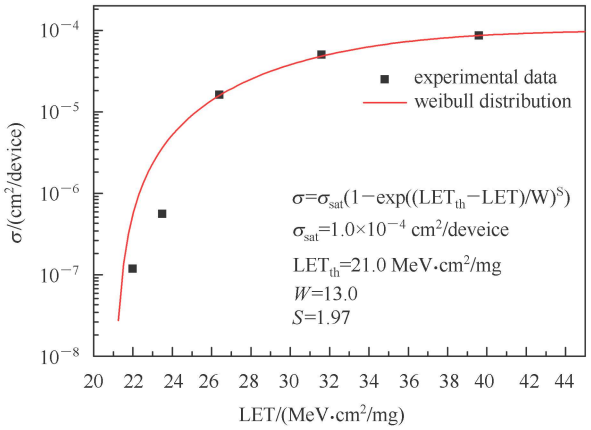

Fig. 5. (color online) SEL cross section of VA160 versus LET (calculated by CREME96).

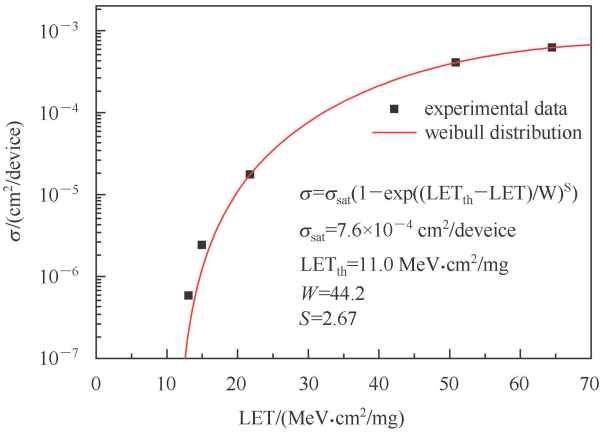

Fig. 6. (color online) SEL cross section of VATA160 versus LET (calculated by CREME96).

The 165-bit configuration register of VATA160 was monitored when the testing was performed at HIRFL. No upset event was observed.

Table 1. Summary of the SEL results.

facility	DUT	ion species	LET/(MeV·cm^2/mg)	fluence/(ions/cm^2)	latch-ups	cross section/(cm^2/device)
HIRFL	VA160	^{84}Kr	20.6	2.23×10^{7}	0	N/A
HIRFL	VA160	^{84}Kr	22.0	3.39×10^{7}	4	1.18×10^{-7}
HIRFL	VA160	^{84}Kr	23.5	5.40×10^{6}	3	5.56×10^{-6}
HIRFL	VA160	^{84}Kr	26.4	1.00×10^{5}	16	1.60×10^{-5}
HIRFL	VA160	^{84}Kr	31.6	3.01×10^{5}	15	4.98×10^{-4}
HIRFL	VA160	^{84}Kr	39.6	1.75×10^{5}	15	8.57×10^{-4}
HI-13	VATA160	^{13}Al	8.4	3.00×10^{7}	0	N/A
HI-13	VATA160	^{32}Cl	13.1	2.75×10^{7}	16	5.82×10^{-7}
HI-13	VATA160	^{32}Cl	15.0	1.00×10^{7}	24	2.40×10^{-6}
HI-13	VATA160	^{22}Ti	21.8	9.22×10^{6}	160	1.73×10^{-5}
HIRFL	VATA160	^{129}Xe	50.9	2.01×10^{5}	82	4.08×10^{-4}
HIRFL	VATA160	^{129}Xe	64.5	1.67×10^{5}	103	6.17×10^{-4}

4 Discussion of hardness assurance and mitigation methods

4.1 Proton SEL rate

The maximum trapped proton energy in the Earth's radiation belts is around 400 MeV, thus the maximum LET of secondary particles produced by the inelastic interactions of protons with Si is about 13.0 MeV·cm^2/mg [10]. Since the SEL LET threshold of VATA160 is about 11.0 MeV·cm^2/mg, proton-induced latch-up should be considered. However, since there is no suitable proton source available for us, an empirical PROFIT method that uses the experimental data of heavy ions to predict the proton rate is adopted instead [11]. Through calculation, the proton SEL rate is about 4.8×10^{-8} /device/day, which is far lower than the heavy ion SEL rate even multiplied by a tenfold calculation error. Hence, the impact of proton SEL is negligible.

4.2 SEL protection method

Over the mission period of 3 years, 52 VA160 chips and 32 VATA160 chips applied in the BGO calorimeter may suffer 4 SEL events and 18 SEL events respectively. Therefore, mitigation methods are strongly recommended. However, it is not practical to change the IC layout or the fabrication process because of cost and schedule. Preventing the chips from damage caused by SEL in the design of the FEE is another possible way.

Though there are at most six VA160 or VATA160 chips mounted on a front-end board, the total fluctuant current is less than 10 mA no matter what mode the chips run in, and the minimum latch-up current that has been observed is at least 25 mA larger than normal operating current. Therefore, a SEL protection circuit with fast response shown in Fig. 7, is developed. A SEL event is identified once the current exceeds a preset threshold, and then the comparison algorithm in the FPGA disables the LDO regulators immediately. The time from current over the threshold to power off is less than 100 μs, which minimizes the burden on the power supply. During the power outage, all control signals from the FPGA are set to ground level as well to avoid the emergence of sneak circuits. After latch-up is removed, the LDO regulators are enabled again to power these chips and the work mode is subsequently restored to the status before power off.

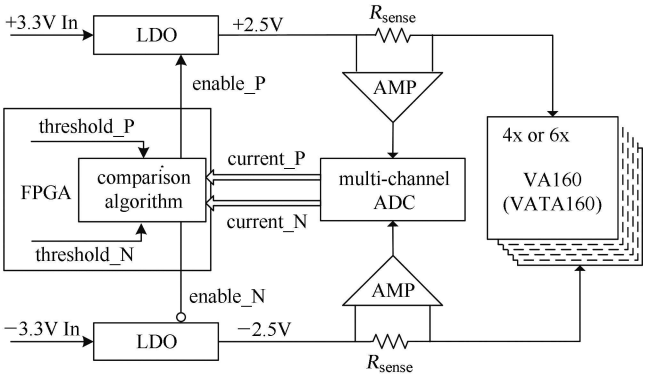

Fig. 7. Simplified schematic of the SEL protection circuit.

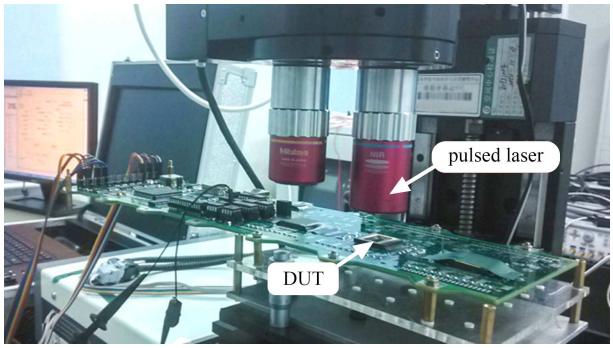

Fig. 8. (color online) The SEL protection circuit in the front-end board was verified by pulsed laser.

A prototype of the front-end board with the protection circuit was verified by pulsed laser, as shown in

Fig. 8. Latch-ups on VA160 or VATA160 were identified and cleared thousands of times without function or performance damage, which sufficiently proved the effectiveness of the protection circuit.

4.3 SEU immune configuration registers

The 165-bit configuration register in the TA part, which maintains the settings for a very long time in orbit, consists of a series of triple-redundancy flip-flops (TRFFs) implemented to avoid loss of information upon SEU events. A sketch showing the principle of a TRFF is shown in Fig. 9. After all bits have been shifted into the DFFs of the serial shift register, the value of each DFF is loaded into the three parallel latches. The output of each TRFF is the logic value that the majority of these latches store.

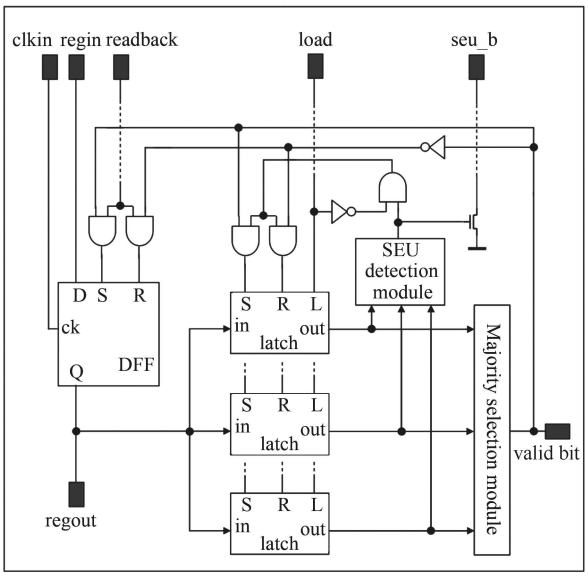

Fig. 9. The structure sketch of a triple-redundancy flip-flop (TRFF).

In case of an upset in a latch, the single event detection module automatically rewrites the three latches with the correct value and sends a flag signal (seu_b) to the external system. A feedback mechanism is provided to load the output of TRFF into the DFF which could be read out through shift operation. During the heavy ion testing performed at HIRFL, the registers were checked the moment a pulse appeared on the seu_b pin. No error was found, which verified that the TRFF is immune to SEU.

4.4 Optimized sequential design

The VA part (or VA160) has two identical 32-bit shift registers that execute the same timing operation shown in Fig. 10. The registers are reset at the beginning and end of each acquisition, which prevents upsets from accumulating and sustaining. As a result, each acquisition is independent. If a register is upset, the worst situation that could happen is that the current acquisition fails. Besides, the chance that the registers of two or more chips are upset simultaneously within an acquisition cycle (less than 1.0 ms) is too rare to happen. According to the physics simulations, temporary abnormality of a chip hardly affects the electromagnetic shower reconstruction in off-line data analysis. Hence, any SEU that occurs on the shift registers is tolerable. Moreover, the independent acquisition makes single event transients (SETs) negligible though the analog circuit occupies the most die area of the ASIC [12].

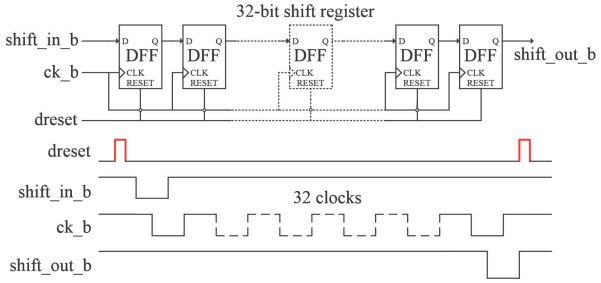

Fig. 10. (color online) The timing diagram of the 32-bit shift register.

5 Conclusion

VA160 and VATA160 chips achieve all the requirements to implement the front-end electronics of the BGO calorimeter except for unknown radiation tolerance, thus SEE tests with pulsed laser and heavy ion were performed. The results showed that the chips are SEL sensitive. The number of expected SEL events on orbit is not negligible since there are 52 VA160 chips and 32 VATA160 chips applied in the calorimeter for more than 3 years. Therefore, an effective SEL protection circuit with fast response, which was sufficiently verified by the pulsed laser test, has been added into the FEE to avoid catastrophic damage caused by SELs. We also conclude that the 165-bit configuration register is immune to SEU, and periodic refreshing removes any possible soft errors caused by ion strikes during long-term acquisition in space. Benefiting from these mitigation methods, the flight model of the BGO calorimeter achieves radiation hardness assurance.

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